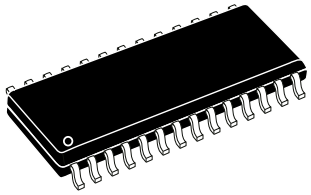
STDRIVE601

Triple half-bridge high-voltage gate driver



SO-28

Features

- High voltage rail up to 600 V
- Driver current capability:
  - STDRIVE601:
    - 200 mA source current @ 25 °C
    - 350 mA sink current @ 25 °C
- dV/dt transient immunity ±50 V/ns
- Gate driving voltage range from 9 V to 20 V
- Overall input-output propagation delay: 85 ns
- Matched propagation delay for all channels
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diodes
- Comparator for fast overcurrent protection
- Smart shutdown function
- Interlocking and deadtime function
- Dedicated Enable pin
- UVLO function on low-side and high-sides

Applications

- 3-phase motor drives
- Inverters

Description

The STDRIVE601 is a high voltage device manufactured with BCD6s offline technology. It is a single-chip with three half-bridge gate drivers for N-channel power MOSFETs or IGBTs suitable for 3-phase applications.

All device outputs can sink and source 350 mA and 200 mA respectively. Prevention from cross conduction is ensured by interlocking and deadtime function.

The device has dedicated input pins for each output and a shutdown pin. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing with control devices. Matched delays between low-side and high-side sections guarantee no cycle distortion and allow high frequency operation.

The STDRIVE601 embeds a comparator featuring advanced SmartSD function also integrated in the device, ensuring fast and effective protection against fault events like overcurrent, overtemperature, etc.

Dedicated UVLO protection on the low-sides and each of the high-side driving sections allow to prevent the power switches from operating in low efficiency or dangerous conditions.

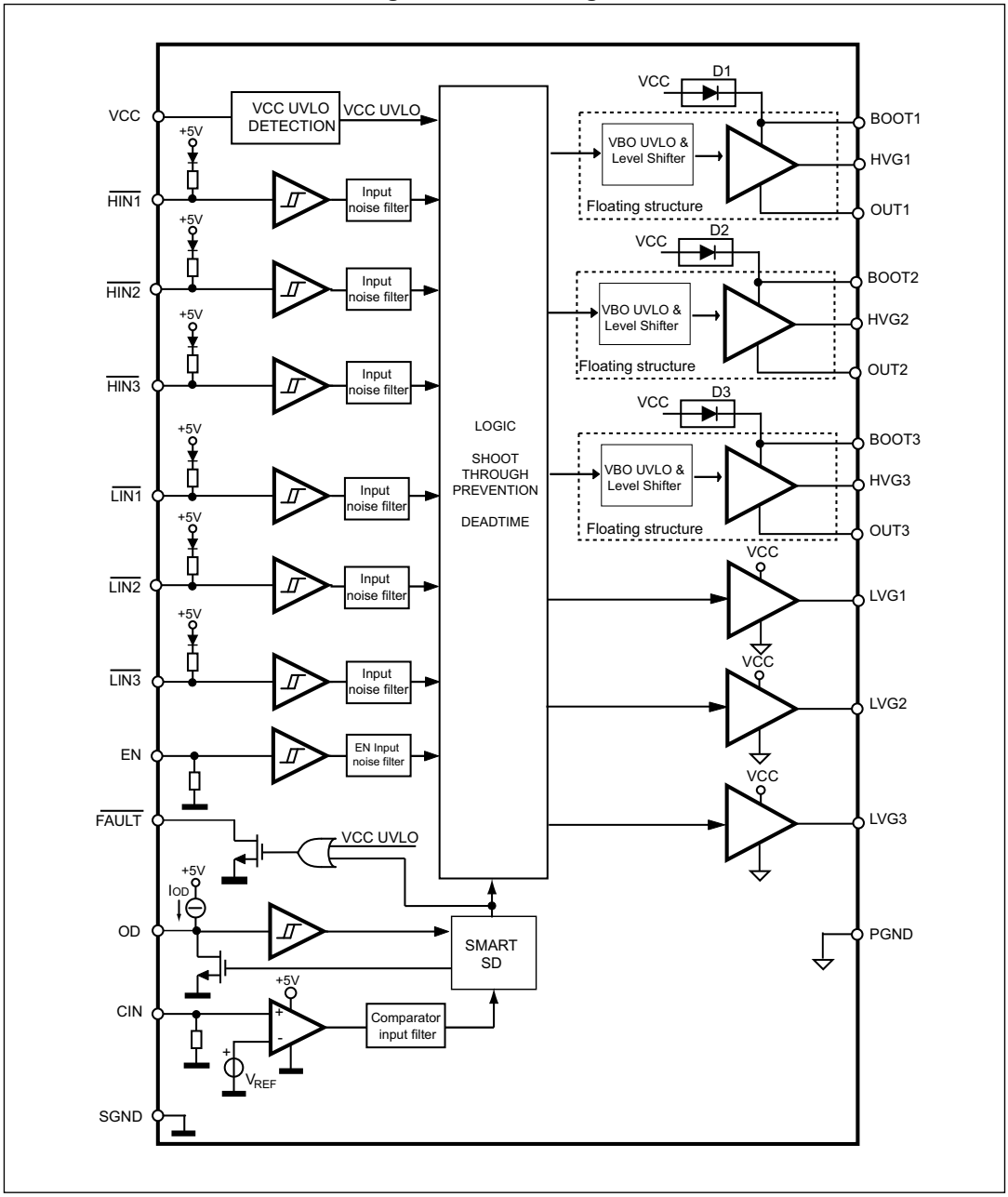
The integrated bootstrap diodes as well as all of the integrated features of this IC make the application PCB design easier, more compact and simple thus reducing the overall bill of material.

The device is available in SO-28 package.

Contents

1 Block diagram

Figure 1. Block diagram



2 Pin description and connection diagram

Figure 2. Pin connection (top view)

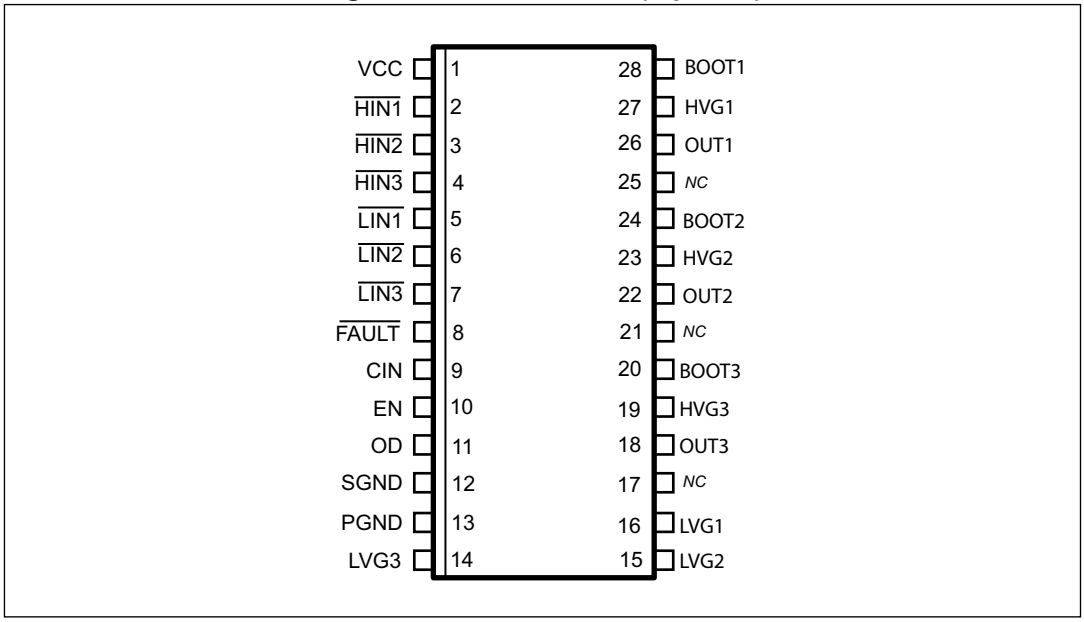


Table 1. Pin description

Pin #	Pin Name	Type	Function
1	VCC	Power Supply	Low-side and logic supply voltage
2	HIN1	Logic Input	High-side driver logic input 1
3	HIN2	Logic Input	High-side driver logic input 2
4	HIN3	Logic Input	High-side driver logic input 3
5	LIN1	Logic Input	Low-side driver logic input 1
6	LIN2	Logic Input	Low-side driver logic input 2
7	LIN3	Logic Input	Low-side driver logic input 3
8	FAULT	OD Output	Fault output
9	CIN	Analog Input	Comparator positive input
10	EN	Logic Input	Enable input, active high
11	OD	OD Output	SmartSD timing Open Drain output, unlatch and restart input
12	SGND	Power Supply	Signal ground
13	PGND	Power Supply	Low-side driver ground
14	LVG3(1)	Analog Output	Low-side driver output 3
15	LVG2(1)	Analog Output	Low-side driver output 2
16	LVG1(1)	Analog Output	Low-side driver output 1
17, 21 25	N.C.	-	Not Connected

Table 1. Pin description (continued)

Pin #	Pin Name	Type	Function
18	OUT3	Power Supply	High-side (floating) common voltage driver 3
19	HVG3(1)	Analog Output	High-side driver output 3
20	BOOT3	Power Supply	Bootstrap supply voltage 3
22	OUT2	Power Supply	High-side (floating) common voltage driver 2
23	HVG2(1)	Analog Output	High-side driver output 2
24	BOOT2	Power Supply	Bootstrap supply voltage 2
26	OUT1	Power Supply	High-side (floating) common voltage driver 1
27	HVG1(1)	Analog Output	High-side driver output 1
28	BOOT1	Power Supply	Bootstrap supply voltage 1

1. The circuit guarantees less than 1 V on the LVG and HVG pins (at I_{sink} = 10 mA), with VCC > 3 V. This allows omitting the “bleeder” resistor connected between the gate and the source of the external MOSFETs normally used to hold the pin low.

3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings(1)

Symbol	Parameter	Min.	Max.	Unit
VCC	Logic supply voltage	-0.3	21	V
V_{PGND}	Low-side driver ground	VCC - 21	VCC + 0.3	V
V_{PS}(2)	Low-side drivers ground	-21	21	V
V_{OUT}	Output voltage	V_{BOOT} - 21	V_{BOOT} + 0.3	V
V_{BOOT}	Bootstrap voltage	- 0.3	620	V
V_{HVG}	High-side gate output voltage	V_{OUT} - 0.3	V_{BOOT} + 0.3	V
V_{LVG}	Low-side gate output voltage	V_{PGND} - 0.3	VCC + 0.3	V
V_{CIN}	Comparator input voltage	- 0.3	20	V
V_i	Logic input voltage(3)	- 0.3	15	V
V_{OD}	OD pin voltage	- 0.3	21	V
V_{FAULT}	FAULT pin voltage	- 0.3	21	V
dV_{OUT}/dt	Common mode transient Immunity		50	V/ns
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-50	150	°C
ESD	Human body model	1		kV

1. Each voltage referred to SGND unless otherwise specified.
2. V_{PS} = PGND - SGND.
3. EN, LINx, HINx.

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient(1)	52	°C/W

1. JEDEC 2s2p PCB in still air.

3.3 Recommended operating conditions

Table 4. Recommended operating conditions(1)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
VCC	Logic supply voltage		9	20	V
V_{LS}(2)	Low-side drivers supply voltage		4	20	V
V_{PS}(3)	Low-side drivers ground		-5	5	V
V_{BO}(4)	Floating supply voltage(4)		8.5	20	V
V_{OUT}	DC Output voltage		-10(5)	580	V
V_{CIN}	Comparator input voltage		0	15	V
V_i	Logic input voltage		0	15	V
V_{OD}	OD pin voltage		0	20	V
V_{FAULT}	FAULT pin voltage		0	20	V
F_{SW}(6)	Maximum switching frequency			800	kHz
PW(7)	Minimum input pulse width		100		ns
T_J	Junction temperature		-40	125	°C

1. Each voltage referred to SGND unless otherwise specified.
2. V_{LS} = VCC - PGND.
3. V_{PS} = PGND - SGND.
4. V_{BO} = BOOT - OUT.
5. VCC = 9 V, LVG off. Logic is operational if V_{BOOT} > 5 V.
6. Actual maximum F_{SW} depends on power dissipation.
7. Pulse width on LIN or HIN pins. See *Figure 3*.

4 Electrical characteristics

HIN is referred to channels HIN1, HIN2, HIN3; LIN is referred to channels LIN1, LIN2, LIN3.

Table 5. Electrical characteristics
(VCC = 15 V; PGND = SGND; TJ = +25 °C, unless otherwise specified)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Low-side section supply							
VCC_{THON}		VCC UVLO turn-on threshold		8	8.5	9	V
VCC_{THOFF}		VCC UVLO turn-off threshold		7.5	8	8.5	V
VCC_{HYS}		VCC UVLO hysteresis		0.4	0.5	0.6	V
I_{QCCU}		VCC undervoltage quiescent supply current	VCC = 7 V; EN = 5 V; CIN = SGND LVG & HVG: OFF		430	744	µA
I_{QCC}		VCC quiescent supply current	EN = 5 V; CIN = SGND LVG & HVG: OFF		950	1450	µA
High-side floating section supply[1]							
V_{BOTHON}		V_{BO} UVLO turn-on threshold		7.5	8	8.5	V
$V_{BOTHOFF}$		V_{BO} UVLO turn-off threshold		7	7.5	8	V
V_{BOHYS}		V_{BO} UVLO hysteresis		0.4	0.5	0.6	V
I_{QBOU}	20 - 18 24 - 22 28 - 26	V_{BO} undervoltage quiescent supply current	VCC = V_{BO} = 6.5 V; EN = 5 V; CIN = SGND LVG OFF; HVG = ON		25	62	µA
I_{QBO}		V_{BO} quiescent supply current	VBO = 15 V EN = 5 V; CIN = SGND LVG OFF; HVG = ON		84	150	µA
I_{LK}		High voltage leakage current	BOOT = HVG = OUT = 620V			15	µA
R_{Dboot}		Bootstrap Diode on resistance			215		Ω

Table 5. Electrical characteristics
(VCC = 15 V; PGND = SGND; TJ = +25 °C, unless otherwise specified) (continued)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Output driving buffers							
I_{SO}	14, 15, 16, 19, 23, 27	High/Low-side source peak current	TJ = 25°C	160	200	300	mA
			Full temperature range(2)	130		350	
I_{SI}		High/Low-side sink peak current	TJ = 25°C	230	350	430	mA
			Full temperature range(2)	200		500	
R_{DSonON}		High/Low-side source RDSon	I = 10 mA	24	35	46	Ω
$R_{DSonOFF}$		High/Low-side sink RDSon	I = 10 mA	11	16	21	Ω
Logic Inputs							
V_{il}	2, 3, 4, 5, 6, 7, 10	Low level logic threshold voltag		0.8		1.4	V
V_{ih}		High level logic threshold voltage		1.8		2.3	V
V_{hyst}	2, 3, 4, 5, 6, 7, 10	Logic input threshold hysteresis		0.8		1.2	V
V_{SSDIh}	11	SmartSD restart threshold		3.5	3.8	4.1	V
V_{SSDIl}		SmartSD unlatch threshold			0.56	0.75	V
I_{LINh}	5, 6, 7	LIN logic “1” input bias current	V_{LINx} = 15 V			1	µA
I_{LINl}		LIN logic “0” input bias current	V_{LINx} = 0 V	28	43	58	µA
I_{HINh}	2, 3, 4	HIN logic “1” input bias current	V_{HINx} = 15 V			1	µA
I_{HINl}		HIN logic “0” input bias current	V_{HINx} = 0	28	43	58	µA
R_{PU_IN}	2, 3, 4, 5, 6, 7	Logic input pull-up resistor		75	100	125	kΩ
I_{ENh}	10	EN logic “1” input bias current	V_{EN} = 15 V	110	150	200	µA
I_{ENl}		EN logic "0" input bias current	V_{EN} = 0 V			1	µA
R_{PD_EN}	10	EN pull-down resistor		75	100	125	kΩ

Table 5. Electrical characteristics
(VCC = 15 V; PGND = SGND; TJ = +25 °C, unless otherwise specified) (continued)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Sense comparator(3) and FAULT							
V_{REF}		Internal voltage reference		410	460	510	mV
C_{INhyst}	9	Comparator input hysteresis		40	70		mV
C_{IN_PD}	9	Comparator input pull-down current	V_{CIN} = 1 V	7	10	13	µA
I_{OD}	11	OD internal current source		2.5	5	7.5	µA
R_{ON_OD}	11	OD On resistance	I_{OD} = 16 mA	19	25	36	Ω
I_{OL_OD}	11	OD low level sink current	V_{OD} = 400 mV	11	16	21	mA
I_{SAT_OD}	11	OD saturation current	V_{OD} = 5 V		95		mA
V_{FLOAT_OD}	11	OD floating voltage level	OD connected only to an external capacitance	4.2	4.7	5	V
R_{ON_F}	8	FAULT ON resistance	I_{FAULT} = 8 mA		50	100	Ω
I_{OL_F}	8	FAULT low level sink current	V_{FAULT} = 400 mV	4	8	12	mA
t_{OD}	11	Comparator propagation delay	Rpu = 100 kΩ to 5 V; voltage step on CIN = 0 to 3.3 V; 50% CIN to 90% OD		350	500	ns
t_{CIN-F}	11	Comparator triggering to FAULT	voltage step on CIN = 0 to 3.3 V; 50% CIN to 90% FAULT		350	500	ns
t_{CINoff}	11	Comparator triggering to high/low-side driver propagation delay	voltage step on CIN = 0 to 3.3 V; 50% CIN to 90% LVG/HVG		360	510	ns
t_{FCIN}	11	Comparator input filter time		200	300	400	ns
SR	11	OD Slew rate	C_L = 1 nF; R_{pu} = 33 kΩ to 5 V; 90% to 10% OD	20	60	100	V/µs

Table 5. Electrical characteristics
(VCC = 15 V; PGND = SGND; TJ = +25 °C, unless otherwise specified) (continued)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics							
t_{on}	2 vs. 27 3 vs 23 4 vs 19	High/Low-side driver turn-on propagation delay	OUT = 0 V BOOT = VCC C_L = 1 nF Vin = 0 to 3.3 V	45	85	120	ns
t_{off}	5 vs. 16 6 vs. 15 7 vs. 14	High/Low-side driver turn-off propagation delay		45	85	120	ns
t_{EN}	10 vs. 14, 15, 16, 19, 23, 27	Enable to high/low-side driver propagation delay		245	385	520	ns
t_{FIN}	2,3,4, 5,6,7	LIN HIN input filter time		30	40	50	ns
t_{FEN}	10	EN input filter time		200	300	400	ns
t_r	14, 15, 16, 19, 23, 27	Rise time	C_L= 1 nF		120	160	ns
t_f		Fall time	C_L= 1 nF		50	75	ns
MT		Delay matching high/low side turn-on/off(4)			0	30	ns
DT		Deadtime	C_L= 1 nF	200	300	400	ns
MDT		Matching deadtime(5)	C_L= 1 nF		0	50	ns

1. V_{BO} = BOOT - OUT.
2. Values provided by characterization, not tested.
3. Comparator is disabled when VCC is in UVLO condition.
4. MT = max. (|ton(LVG) - toff(LVG)|, |ton(HVG) - toff(HVG)|, |toff(LVG) - ton(HVG)|, |toff(HVG) - ton(LVG)|).
5. MDT = | DTLH - DTHL |, refer to *Figure 5*.

Figure 3. Propagation delay timing definition

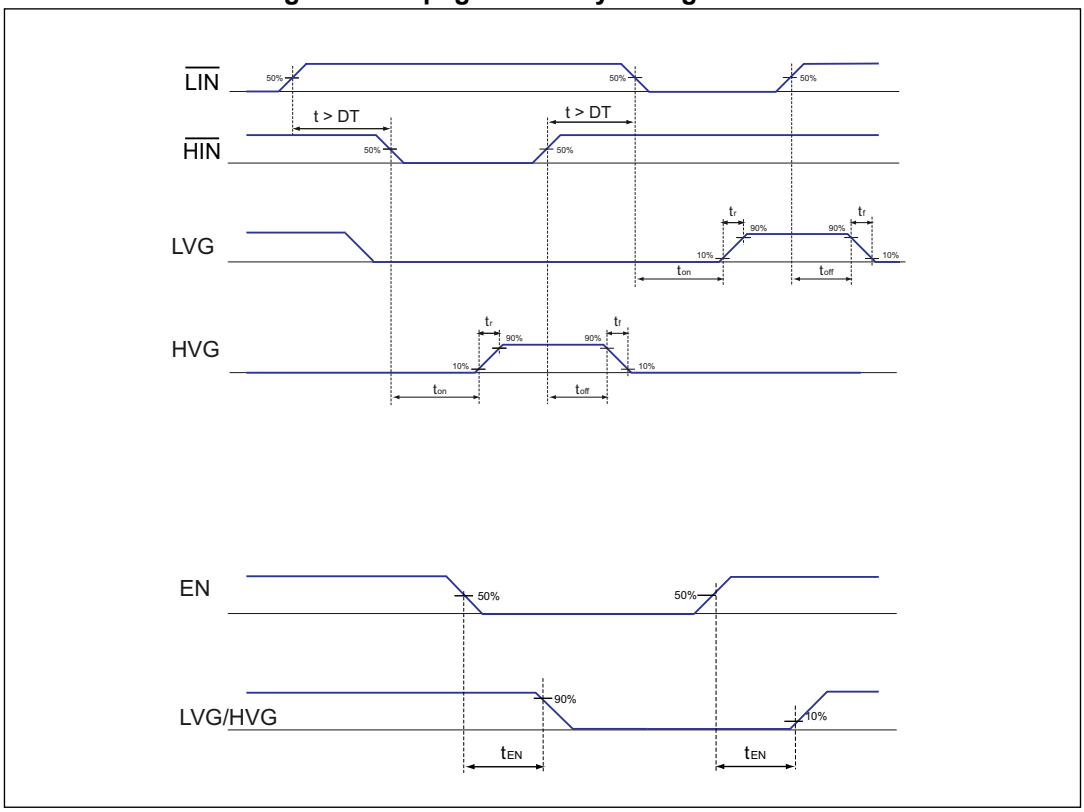


Figure 4. Deadtime timing definitions

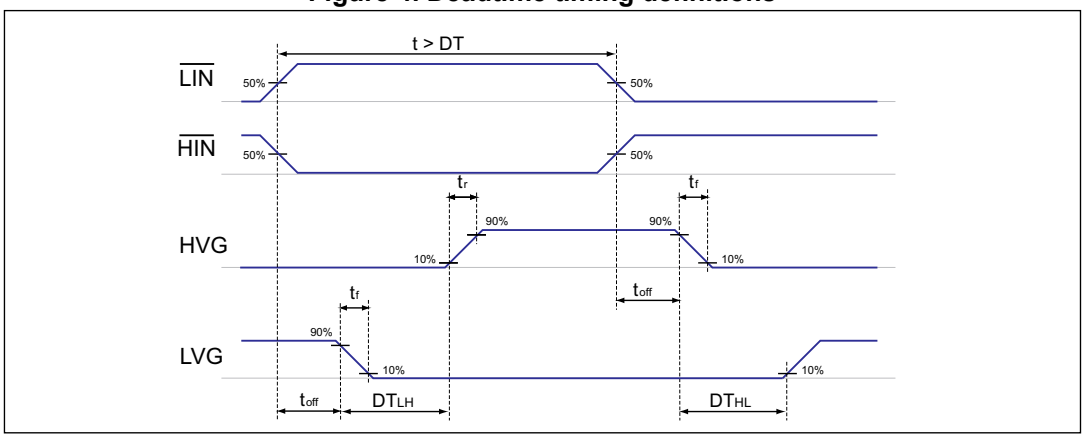
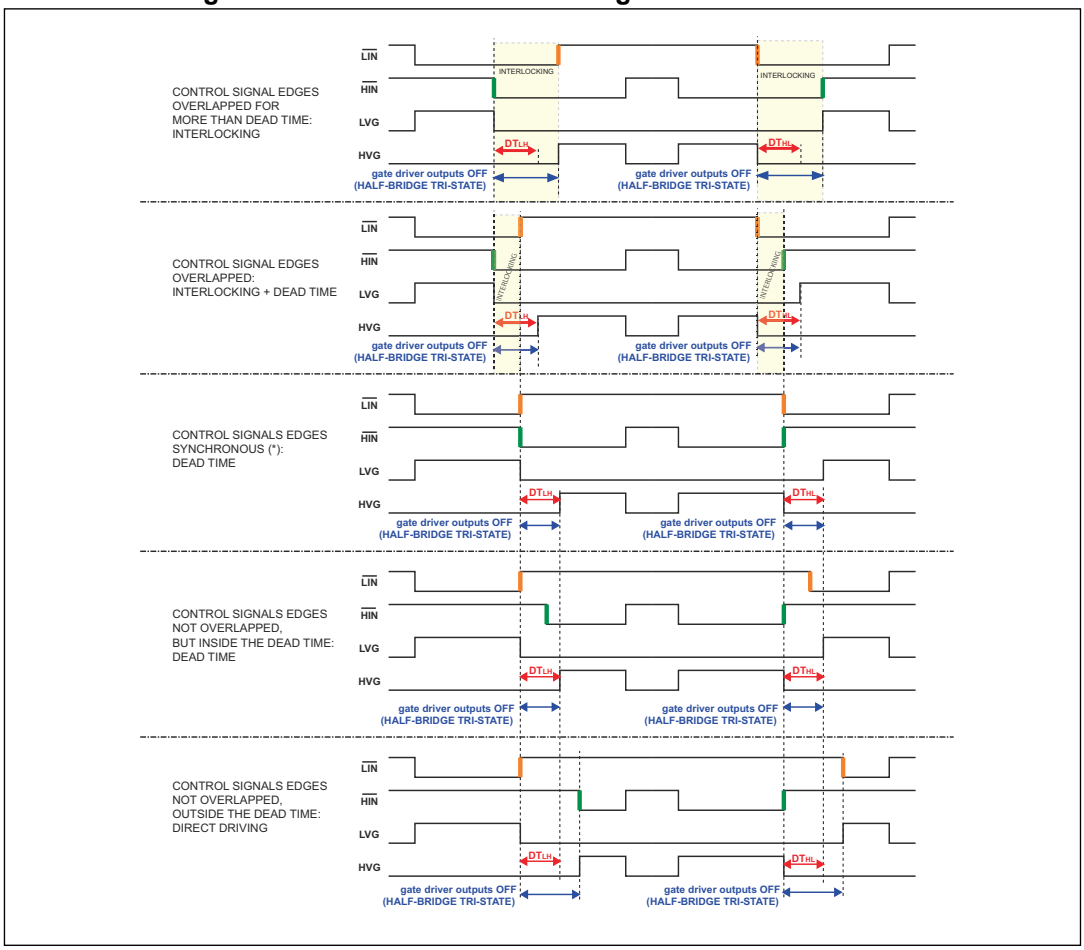


Figure 5. Deadtime and interlocking waveforms definition



5 Functional description

5.1 Inputs and outputs

The devices are controlled through the following logic inputs:

- EN: Enable input, active high;
- LIN: low-side driver inputs, active low;
- HIN: high-side driver inputs, active low.

Table 6. Inputs truth table (applicable when device is not in UVLO or SmartSD protection)

	Input pins			Output pins	
	EN	**$\overline{\text{LIN}}$**	**$\overline{\text{HIN}}$**	**LVG**	**HVG**
	L	X	X	Low	Low
	H	H	H	Low	Low
	H	L	H	**High**	Low
	H	H	L	Low	**High**
Interlocking	H	L	L	Low	Low

The FAULT and OD pins are open-drain outputs.

The FAULT signal is set low in case VCC UVLO is detected, or in case the SmartShutDown comparator triggers an event. It is only used to signal a UVLO or SmartSD activation to external circuits, and its state does not affect the behavior of other functions or circuits inside the driver. The OD behavior is explained in *Section 5.5*.

When EN is set low, gate driver outputs are forced low and assure low impedance.

5.2 Deadtime

The deadtime feature, in companion with interlocking feature, guarantees that driver outputs of the same channel are not high simultaneously and at least a DT time passes between the turn-off of one driver's output and the turn-on of the companion output of the same channel. If a deadtime longer than the internal DT is applied to LIN and HIN inputs by the external controller, the internal DT is ignored and the outputs follow the deadtime determined by the inputs.

Refer to *Figure 4* for the dead time and interlocking waveforms.

5.3 VCC UVLO protection

Undervoltage protection is available on VCC and BOOT supply pins. In order to avoid intermittent operation, a hysteresis set the turn-off threshold with respect to the turn-on threshold.

When VCC voltage goes below VCC_{THOFF} threshold all the outputs are switched off, both LVG and HVG. When VCC voltage reaches VCC_{THON} threshold the driver returns to normal operation and sets the LVG outputs according to actual input pins status; HVG is also set according to input pin status if the corresponding V_{BO} section is not in UVLO condition.

The FAULT output is kept low when VCC is in UVLO condition. The following figures show some examples of typical operation conditions.

Figure 6. VCC power ON and UVLO, LVG timing(a)

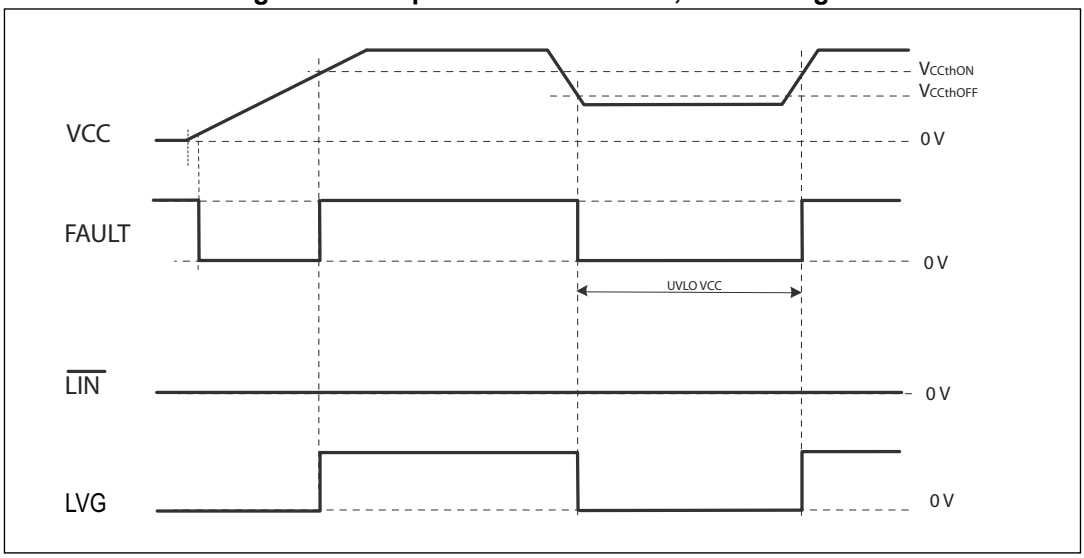
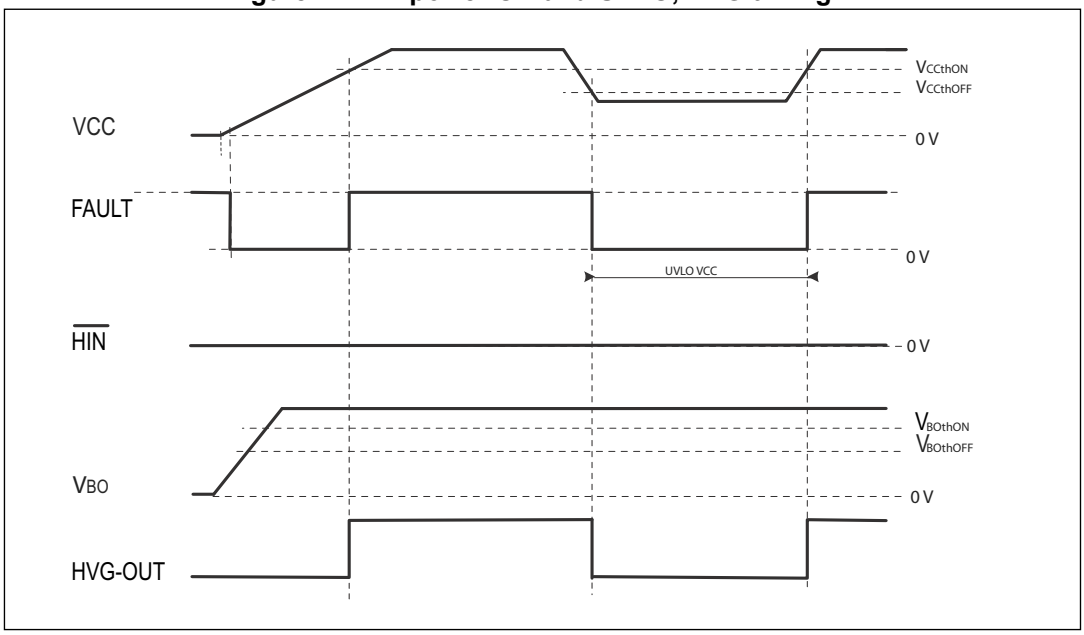


Figure 7. VCC power ON and UVLO, HVG timing(a)



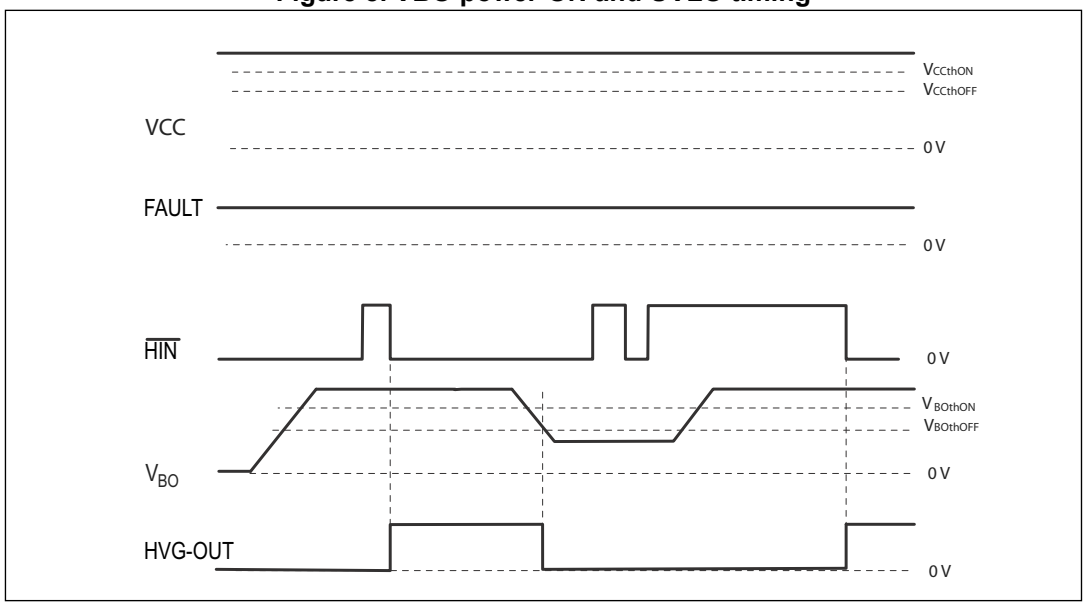
a. Fault pin connected to external pull-up.

5.4 VBO UVLO protection

Dedicated undervoltage protection is available on each bootstrap section between BOOTx and OUTx supply pins. In order to avoid intermittent operation, a hysteresis sets the turn-off threshold with respect to the turn-on threshold.

When V_{BO} voltage goes below $V_{BOTHOFF}$ threshold, the HVG output of corresponding bootstrap section is switched off. When V_{BO} voltage reaches V_{BOTHON} threshold device returns to normal operation and the output remains off up to the next input pins transition that requests HVG to turn on.

Figure 8. VBO power-ON and UVLO timing



5.5 Comparator and smart shutdown

These devices integrate a comparator committed to the fault protection function, thanks to the SmartShutDown (SmartSD) circuit.

The SmartSD architecture allows immediate turn-off of the gate driver outputs in the case of overload or overcurrent condition, by minimizing the propagation delay between the fault detection event and the actual output switch-off. In fact, the time delay between the fault detection and the output turn-off is not dependent on the value of the external components connected to the OD pin, which are only used to set the duration of disable time after the fault.

This provides the possibility to increase the duration of the *output disable time* after the fault event up to very large values without increasing the delay time of the protection. The duration of the disable time is determined by the values of the external capacitor C_{OD} and of the optional pull-up resistor connected to OD pin.

The comparator has an internal voltage reference V_{REF} connected to the inverting input, while the non-inverting input is available on the CIN pin. The comparator's CIN input can be connected to an external shunt resistor in order to implement a fast and simple overcurrent protection function. The output signal of the comparator is filtered from glitches shorter than t_{FCIN} and then fed to the SmartSD logic.

If the impulse on CIN pin is higher than V_{REF} and wider than t_{FCIN}, the SmartSD logic is triggered and immediately sets all of the driver outputs to low-level (OFF).

At the same time, FAULT is forced low to signal the event (for example to an MCU input) and OD starts to discharge the external C_{OD} capacitor used to set the duration of the output disable time of the fault event.

The FAULT pin is released and driver outputs restart following the input pins as soon as the *output disable time* expires.

The overall disable time is composed of two phases:

- The *OD unlatch time* (t_1 in *Figure 9*), which is the time required to discharge C_{OD} capacitor down to V_{SSDl} threshold. The discharge starts as soon as the SmartSD comparator is triggered.
- The *OD restart time* (t_2 in *Figure 9*), which is the time required to recharge the C_{OD} capacitor up to the V_{SSDh} threshold. The recharge of C_{OD} starts when the OD internal MOSFET is turned-off, which happens when the fault condition has been removed (CIN < V_{REF} - C_{INhyst}) and the voltage on OD reaches the V_{SSDl} threshold. This time normally covers most of the overall output disable time.

If no external pull-up is connected to OD, the external C_{OD} capacitor is discharged with a time constant defined by C_{OD} and the internal MOSFET's characteristic (Equation 1), and the *Restart time* is determined by the internal current source I_{OD} and by C_{OD} (Equation 2).

Equation 1

$$t_1 \cong R_{ON\_OD} \cdot C_{OD} \cdot ln\left(\frac{V_{OD}}{V_{SSDl}}\right)$$

Equation 2

$$t_2 \cong \frac{C_{OD} \cdot V_{SSDh}}{I_{OD}} \cdot ln\left(\frac{V_{SSDl} - V_{OD}}{V_{SSDh} - V_{OD}}\right)$$

In case the OD pin is connected to VCC by an external pull-up resistor R_{OD_ext}, the OD discharge time is determined by the external network R_{OD_ext} C_{OD} and by the internal MOSFET's R_{ON_OD} (*Equation 3*), while the *Restart time* is determined by current in R_{OD_ext} (*Equation 4*).

Equation 3

$$t_1 \cong C_{OD} \cdot (R_{OD\_ext} // R_{ON\_OD}) \cdot ln\left(\frac{V_{OD} - V_{on}}{V_{SSDl} - V_{on}}\right)$$

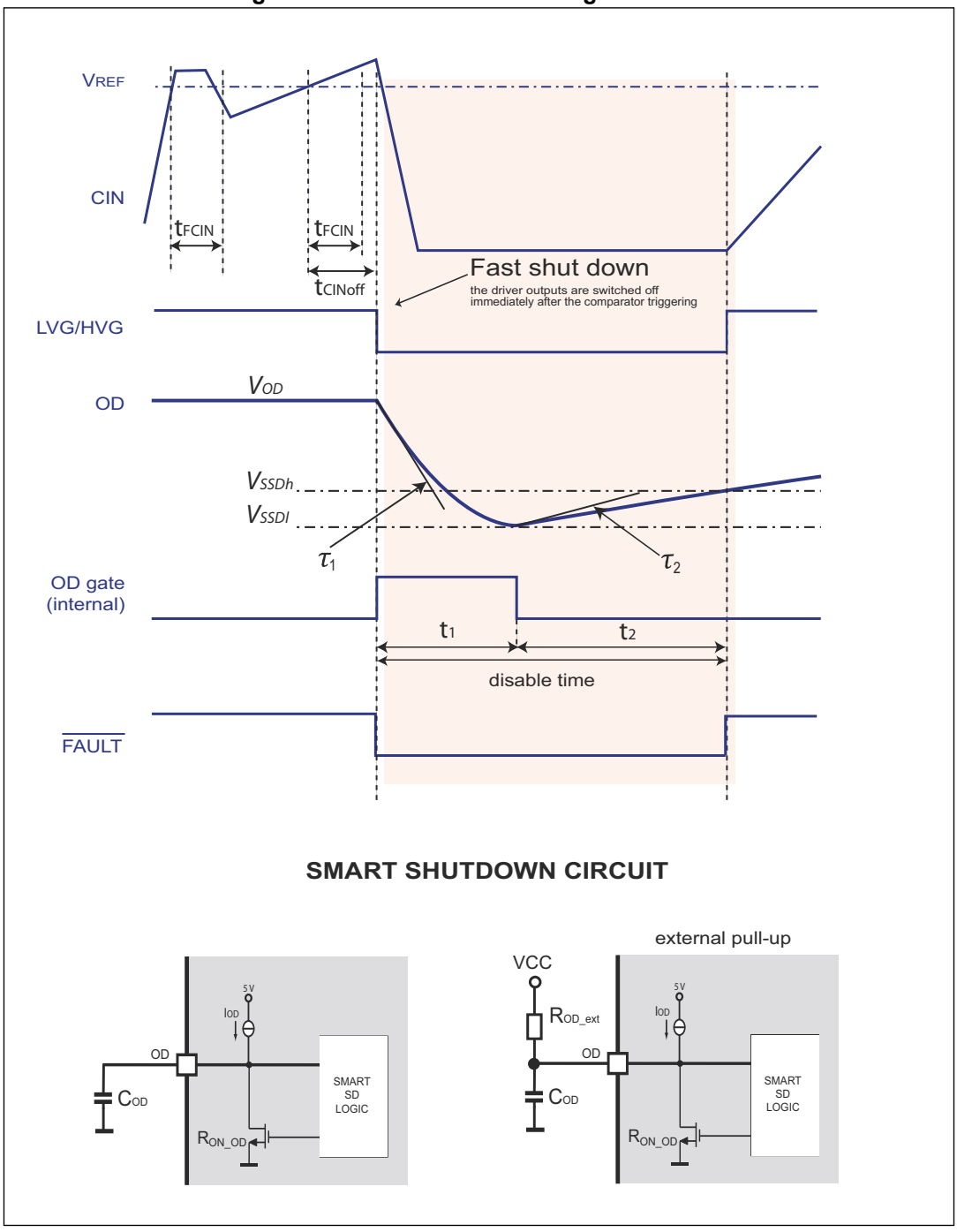
Equation 4

$$t_1 \cong C_{OD} \cdot R_{OD\_ext} \cdot ln\left(\frac{V_{SSDl} - V_{OD}}{V_{SSDh} - V_{OD}}\right)$$

where

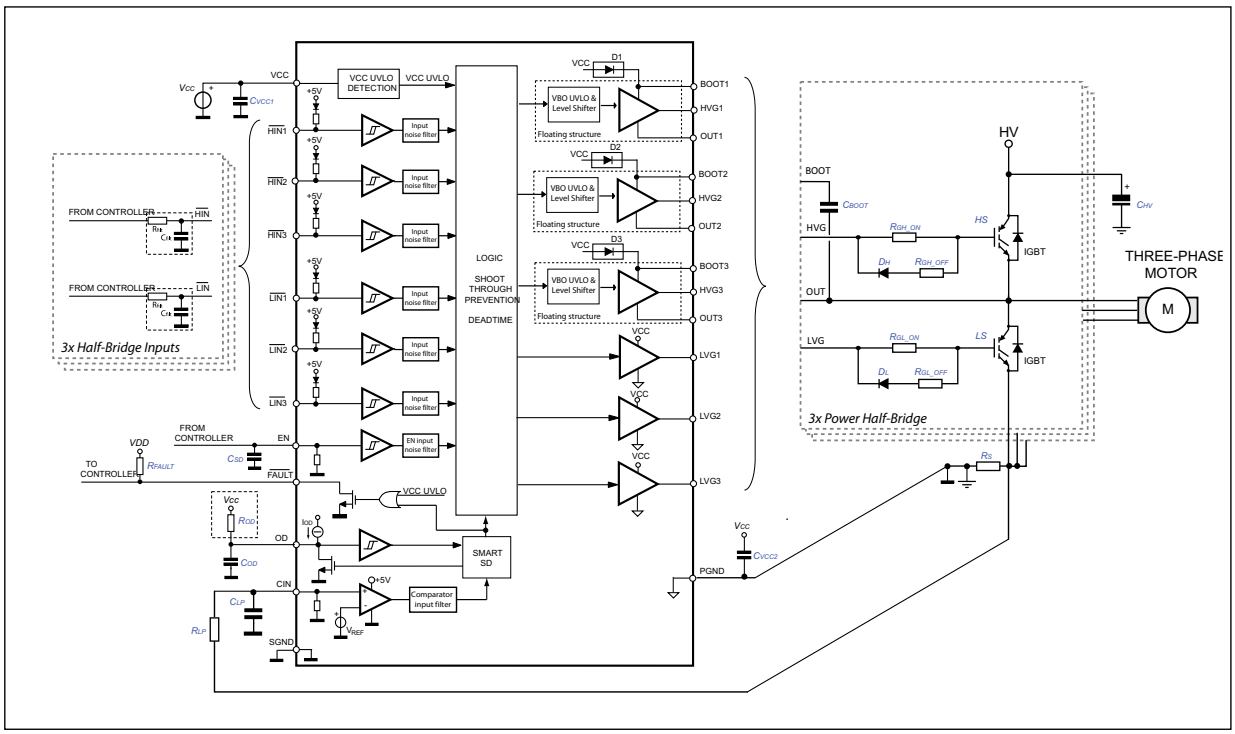
$$V_{on} = \frac{R_{ON\_OD}}{R_{OD\_ext} + R_{ON\_OD}} \cdot VCC; \qquad V_{OD} = VCC$$

Figure 9. Smart shutdown timing waveforms



6 Typical application diagram

Figure 10. Typical application diagram



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 SO-28 package information

Table 7. SO-28 package dimensions

Dim.	Mm			NOTES
	Min.	Typ.	Max.	
A	2.35		2.65	
A1	0.10		0.30	
B	0.33		0.51	
C	0.23		0.32	
D	17.70		18.10	
E	7.40		7.60	
e		1.27		
H	10.00		10.65	
h	0.25		0.75	
L	0.40		1.27	
k	0		8	DEGREES
ddd			0.10	

Figure 11. SO-28 mechanical data

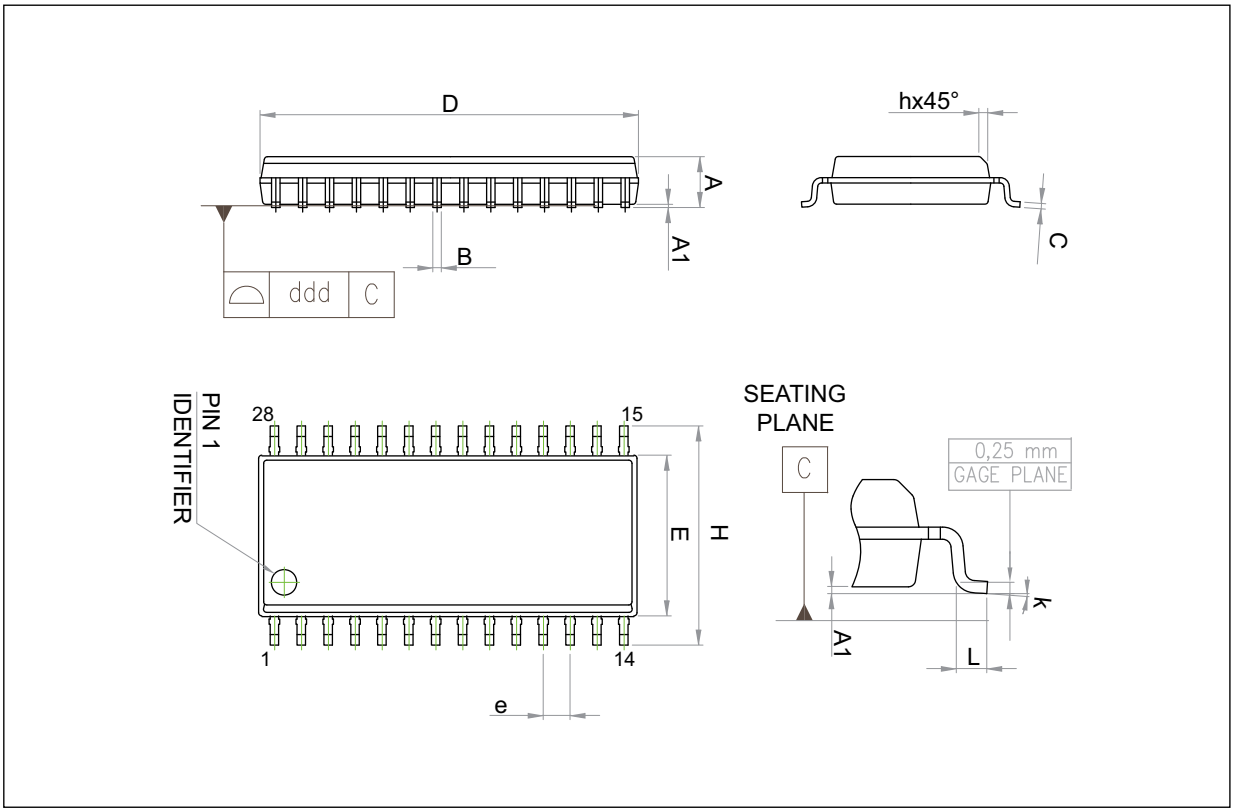
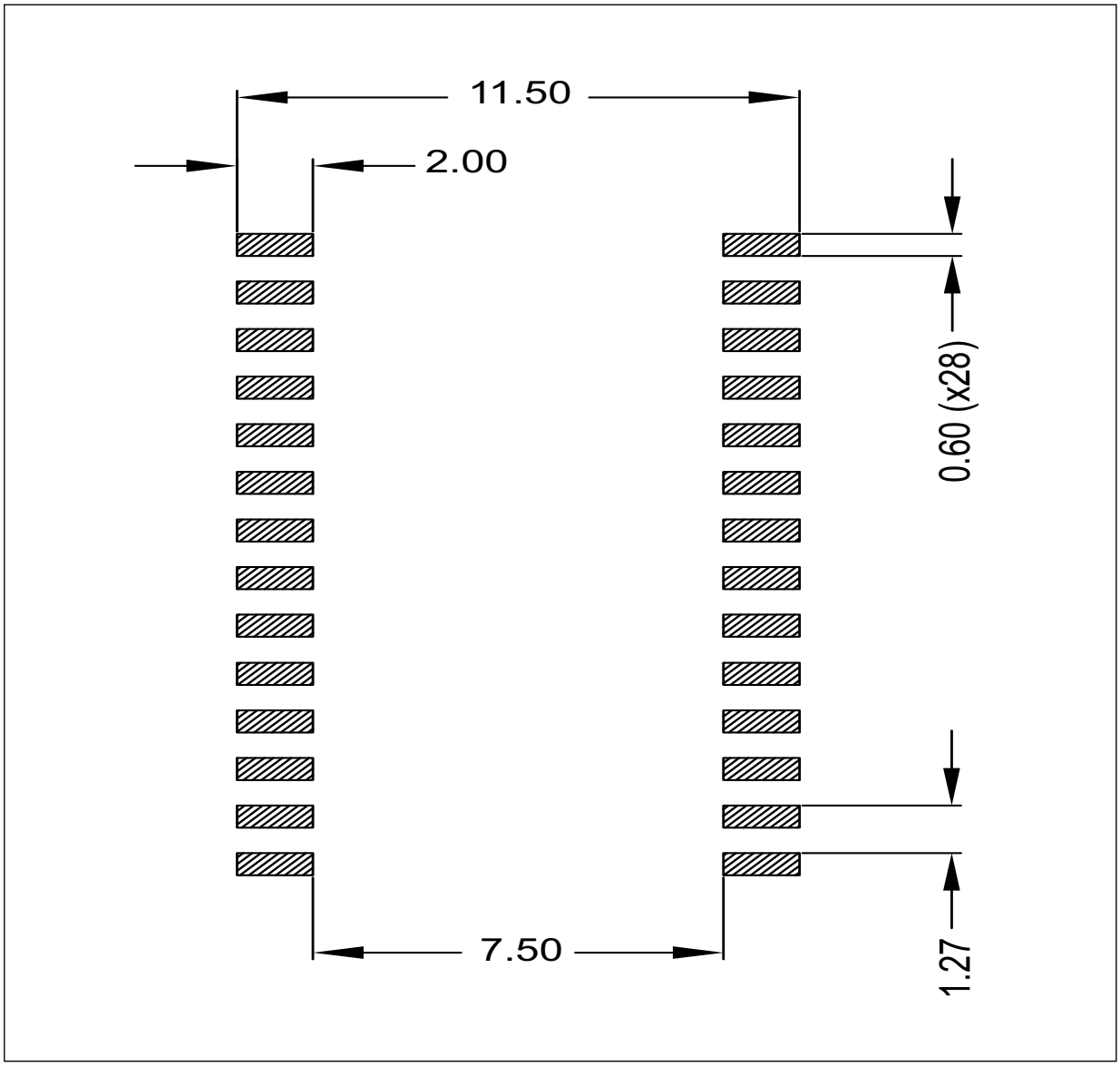


Figure 12. SO-28 suggested land pattern



8 Ordering information

Table 8. Order codes

Order code	Package	Marking	Packaging
STDRIVE601	SO-28	STDRV601	Tube
STDRIVE601TR	SO-28	STDRV601	Tape and reel

9 Revision history

Table 9. Document history

Date	Revision	Changes
21-May-2019	1	Initial release.

Mouser Electronics

Authorized Distributor

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STMicroelectronics:

STDRIVE601TR STDRIVE601