0.3 GHz to 6 GHz, 35 W, GaN Power Amplifier

Data Sheet **HMC8205BF10**

FEATURES

High P_{SAT}: 46 dBm
High power gain: 20 dB
High PAE: 38%
Instantaneous bandwidth: 0.3 GHz to 6 GHz
Supply voltage: V_{DD} = 50 V at 1300 mA
10-lead LDCC package

APPLICATIONS

Military jammers
Commercial and military radar
Power amplifier stage for wireless infrastructure
Test and measurement equipment

FUNCTIONAL BLOCK DIAGRAM

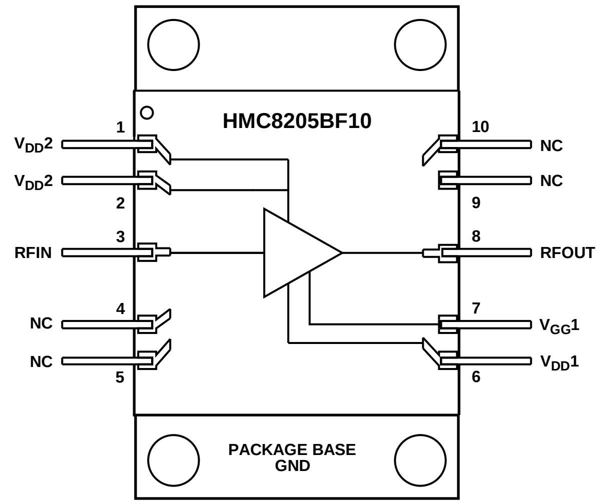

Figure 1.

GENERAL DESCRIPTION

The HMC8205BF10 is a gallium nitride (GaN) broadband power amplifier delivering 45.5 dBm (35 W) with 38% power added efficiency (PAE) across an instantaneous bandwidth of 0.3 GHz to 6 GHz. No external matching is required to achieve full band operation. Additionally, no external inductor is required to bias the amplifier. Also, dc blocking capacitors for the RFIN and RFOUT pins are integrated into the HMC8205BF10.

The HMC8205BF10 is ideal for pulsed or continuous wave (CW) applications, such as military jammers, wireless infrastructure, radar, and general-purpose amplification.

The HMC8205BF10 amplifier is a 10-lead ceramic leaded chip carrier (LDCC).

Rev. C Document Feedback

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Tel: 781.329.4700

Technical Support **www.analog.com**

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5/2017—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, V_{DD} = 50 V, I_{DQ} = 1300 mA, frequency range = 0.3 GHz to 3 GHz.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.3		3	GHz	
GAIN						
Small Signal Gain		23	26		dB	
Gain Flatness			±2		dB	
RETURN LOSS						
Input			13		dB	
Output			12		dB	
POWER						
4 dB Compressed Power	P_{4dB}	39	45		dBm	
Saturated Output Power	P_{SAT}		46		dBm	
Power Gain for P_{SAT}			20		dB	
Power Added Efficiency	PAE		38		%	
TOTAL SUPPLY CURRENT	I_{DQ}		1300		mA	
SUPPLY VOLTAGE	V_{DD}	28	50	55	V	

T_A = 25°C, V_{DD} = 50 V, I_{DQ} = 1300 mA, frequency range = 3 GHz to 6 GHz.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		3		6	GHz	
GAIN						
Small Signal Gain		25	28		dB	
Gain Flatness			±2		dB	
RETURN LOSS						
Input			10		dB	
Output			7		dB	
POWER						
4 dB Compressed Power	P_{4dB}	39	45		dBm	
Saturated Output Power	P_{SAT}		46		dBm	
Power Gain for P_{SAT}			19		dB	
Power Added Efficiency	PAE		35		%	
TOTAL SUPPLY CURRENT	I_{DQ}		1300		mA	
SUPPLY VOLTAGE	V_{DD}	28	50	55	V	

ABSOLUTE MAXIMUM RATINGS

This device is not surface mountable and is not intended nor suitable to be used in a solder reflow process. This device must not be exposed to ambient temperatures above 150°C.

Table 3.

Parameter	Rating
Drain Bias Voltage (V_{DD})	60 V dc
Gate Bias Voltage ($V_{GG}1$)	−8 V to 0 V dc
Radio Frequency (RF) Input Power (RFIN)	35 dBm
Continuous Power Dissipation (P_{DISS}) (T = 85°C) (Derate 636 mw/°C Above 85°C)	89.4 W
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−40°C to +85°C
Human Body Model (HBM) Electrostatic Discharge (ESD) Sensitivity	375 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
EJ-10-1	1.57	°C/W

Table 5. Reliability Information

Parameter	Temperature (°C)
Junction Temperature to Maintain 1,000,000 Hour Mean Time to Failure (MTTF)	225
Nominal Junction Temperature (T = 85°C, V_{DD} = 50 V)	187

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

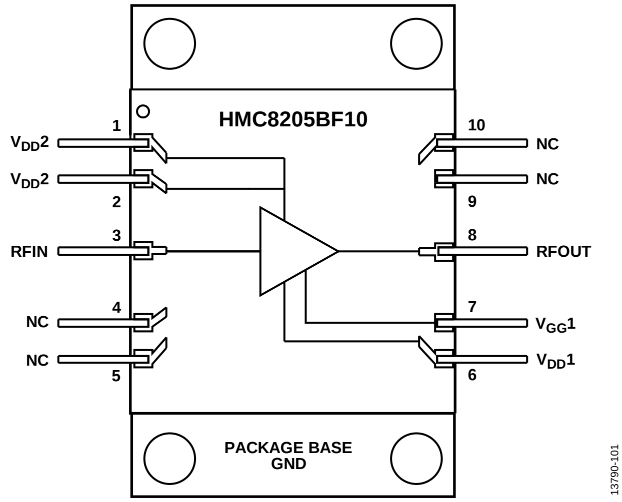

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2	$V_{DD}2$	Drain Bias for Second Stage of Amplifier. See Figure 3 for the $V_{DD}2$ interface schematic.
3	RFIN	RF Input (RFIN). It is ac-coupled and internally matched to 50 Ω. See Figure 4 for the RFIN interface schematic.
4, 5, 9, 10	NC	No Internal Connection.
6	$V_{DD}1$	Drain Bias for First Stage of Amplifier. See Figure 5 for the $V_{DD}1$ interface schematic.
7	$V_{GG}1$	Gate Control for Second Stage of Amplifier. See Figure 6 for the $V_{GG}1$ interface schematic.
8	RFOUT	RF Output (RFOUT). It is ac-coupled and internally matched to 50 Ω. See Figure 7 for the RFOUT interface schematic.
Package Base	GND	Package Base. The package base must be connected to RF/dc ground. See Figure 8 for the GND Interface schematic.

INTERFACE SCHEMATICS

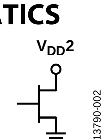

Figure 3. $V_{DD}2$ Interface

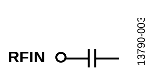

Figure 4. RFIN Interface

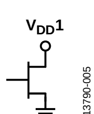

Figure 5. $V_{DD}1$ Interface

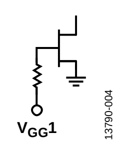

Figure 6. $V_{GG}1$ Interface

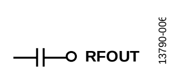

Figure 7. RFOUT Interface

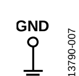

Figure 8. GND Interface

TYPICAL PERFORMANCE CHARACTERISTICS

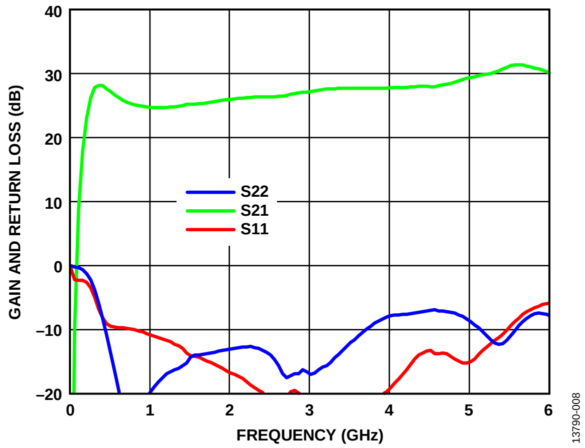

Figure 9. Gain and Return Loss vs. Frequency

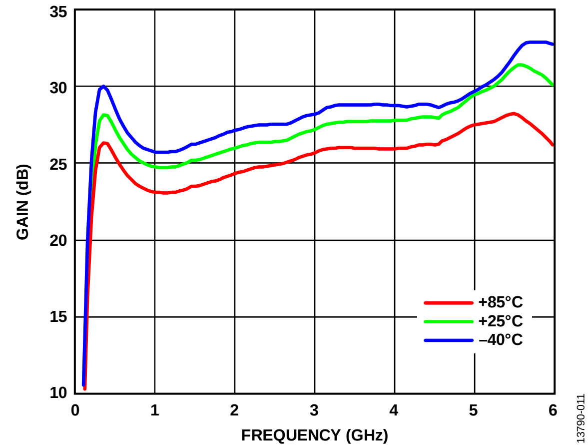

Figure 12. Gain vs. Frequency at Various Temperatures

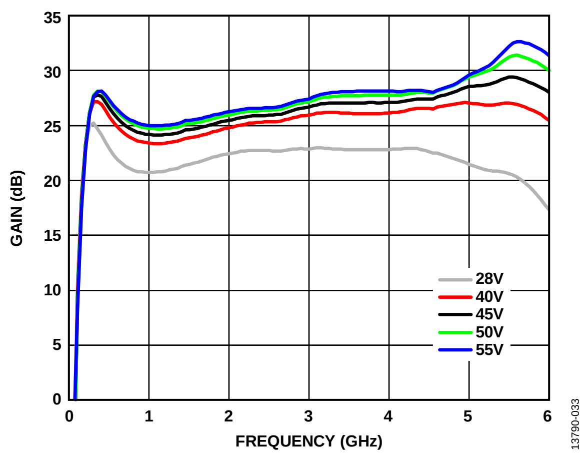

Figure 10. Gain vs. Frequency at Various Supply Voltages

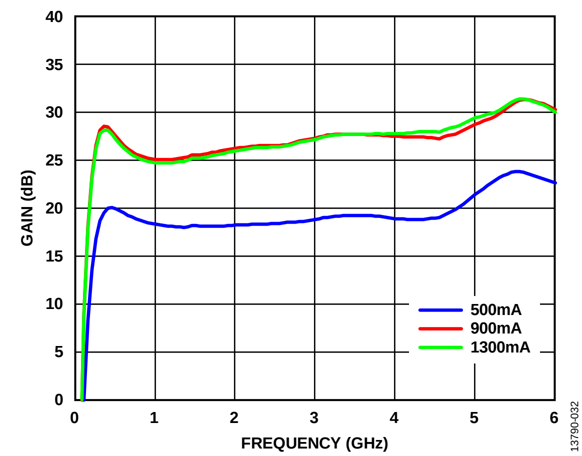

Figure 13. Gain vs. Frequency at Various Supply Currents

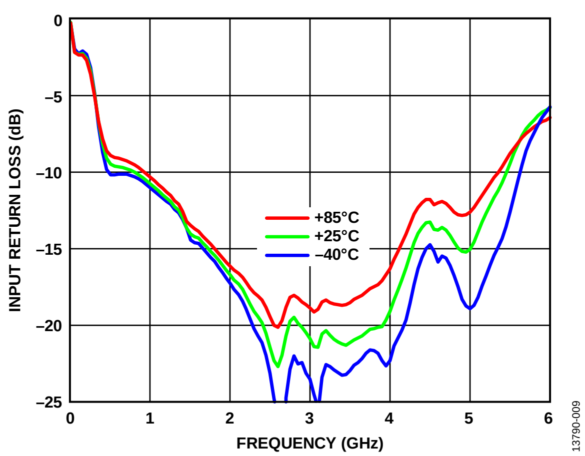

Figure 11. Input Return Loss vs. Frequency at Various Temperatures

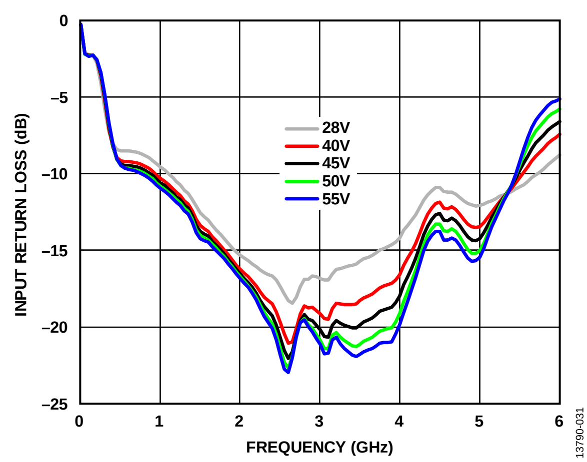

Figure 14. Input Return Loss vs. Frequency at Various Supply Voltages

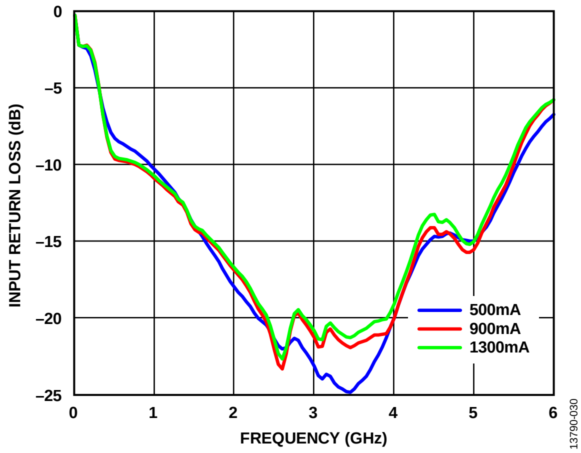

Figure 15. Input Return Loss vs. Frequency at Various Supply Currents

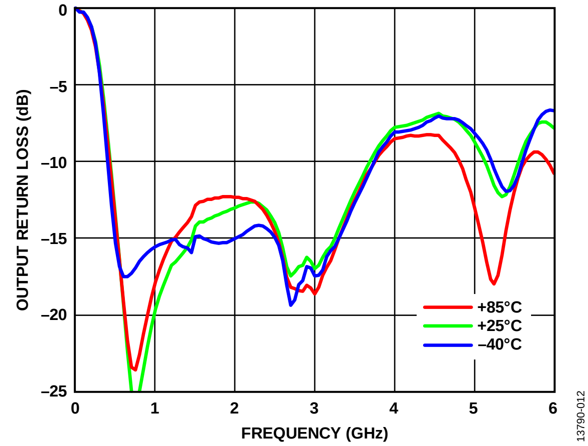

Figure 18. Output Return Loss vs. Frequency at Various Temperatures

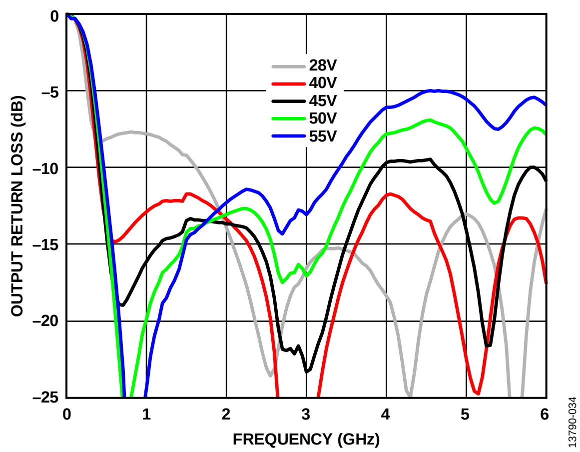

Figure 16. Output Return Loss vs. Frequency at Various Supply Voltages

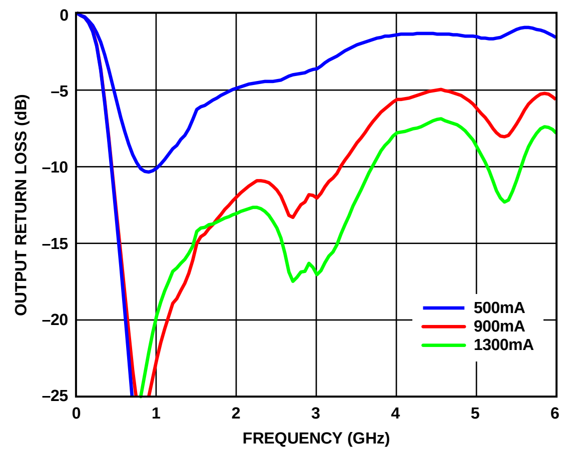

Figure 19. Output Return Loss vs. Frequency at Various Supply Currents

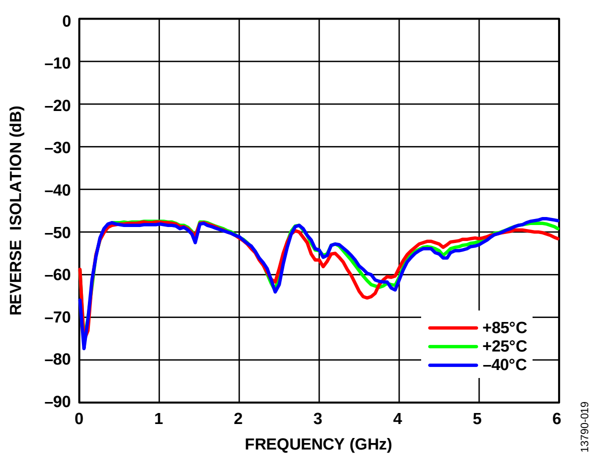

Figure 17. Reverse Isolation vs. Frequency at Various Temperatures

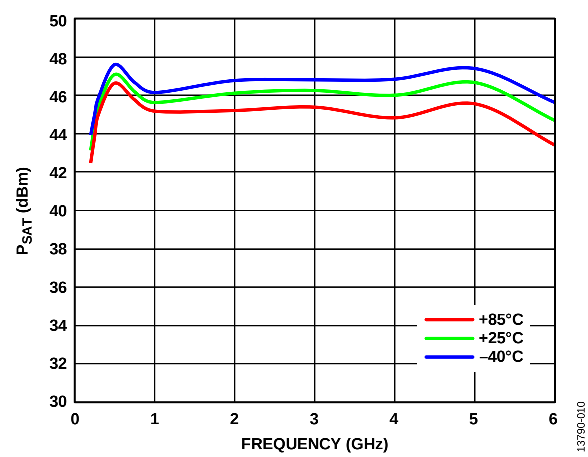

Figure 20. P_{SAT} vs. Frequency at Various Temperatures; Input Power Set to 26 dBm

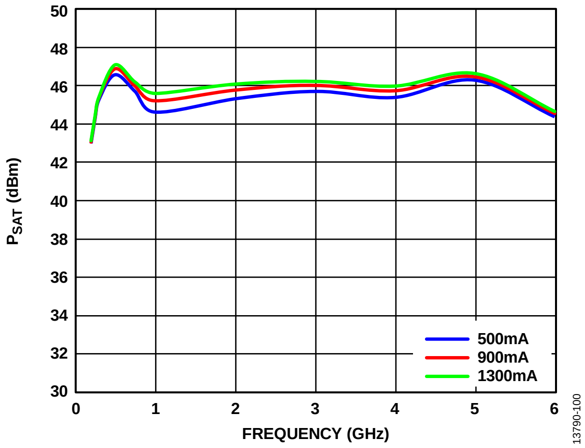

Figure 21. P_{SAT} vs. Frequency at Various Supply Currents; Input Power Set to 26 dBm

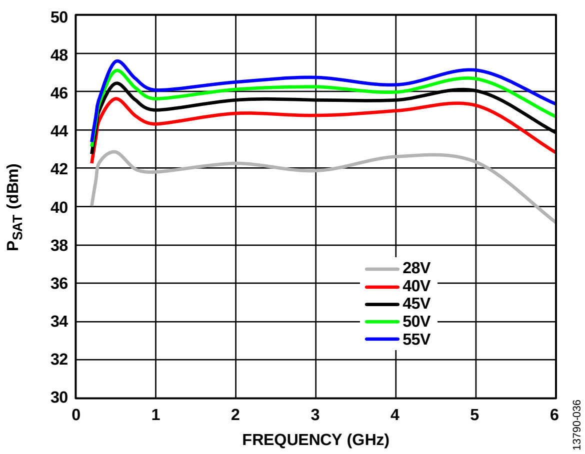

Figure 22. P_{SAT} vs. Frequency at Various Supply Voltages; Input Power Set to 26 dBm

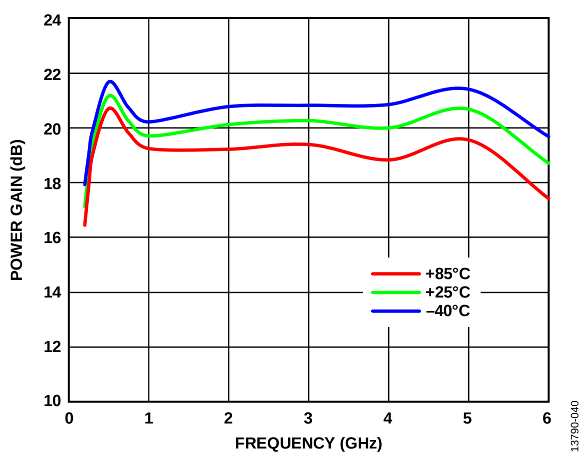

Figure 23. Power Gain vs. Frequency at Various Temperatures; Input Power Set to 26 dBm

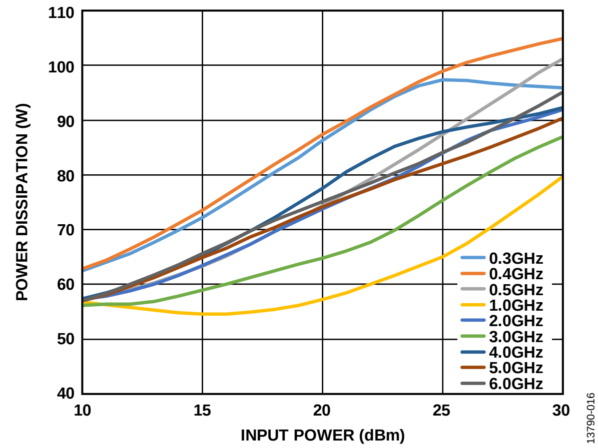

Figure 24. Power Dissipation vs. Input Power at Various Frequencies

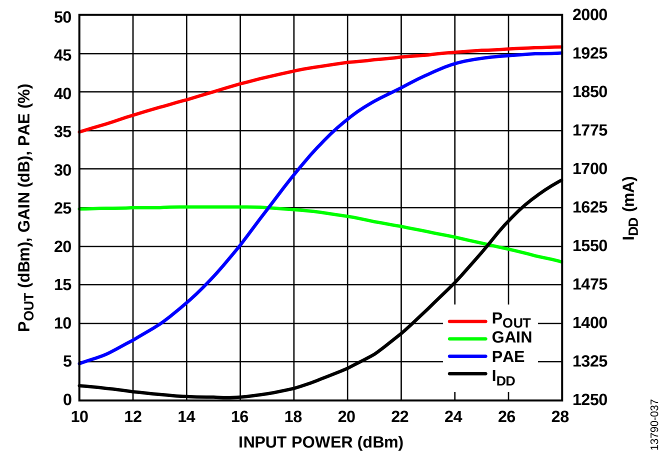

Figure 25. Output Power (P_{OUT}), Gain, PAE, and Total Supply Current (I_{DD}) with RF Power Applied vs. Input Power at 1 GHz

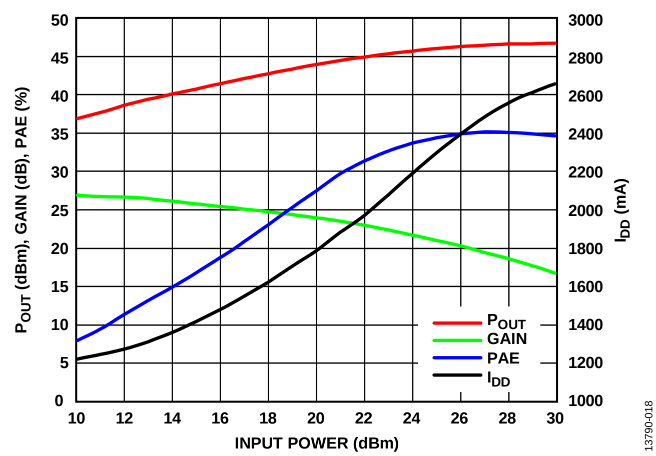

Figure 26. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at 3 GHz

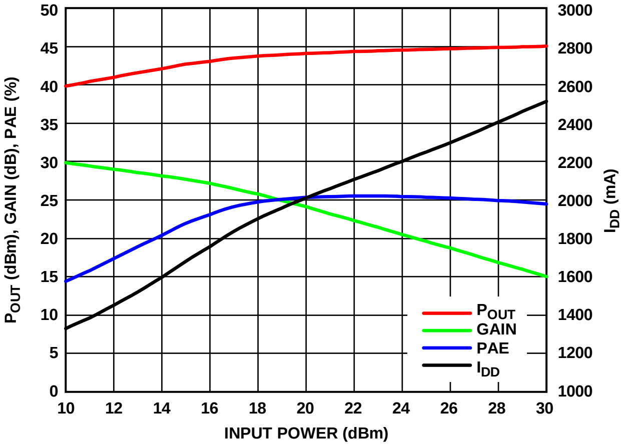

Figure 27. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at 6 GHz

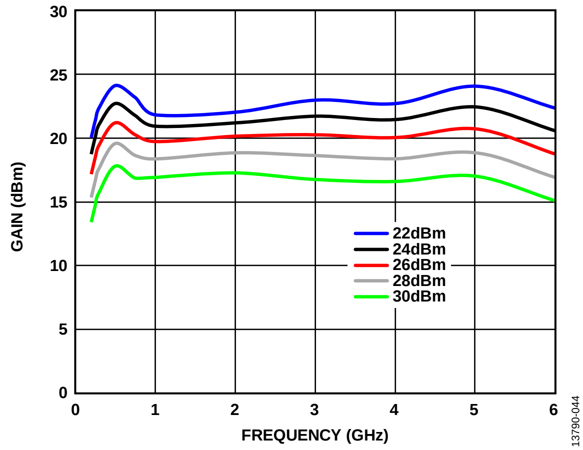

Figure 30. Gain vs. Frequency at Various Input Powers

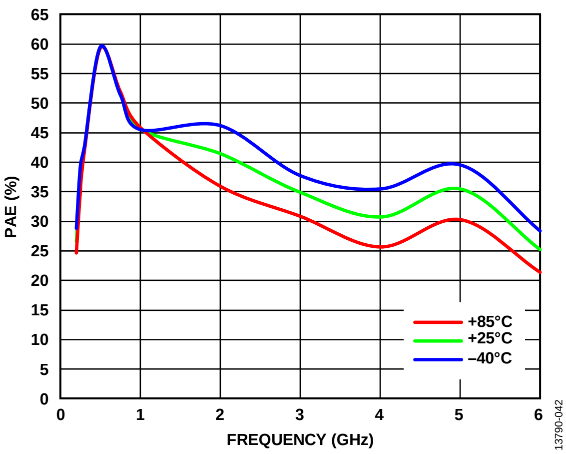

Figure 28. PAE vs. Frequency at Various Temperatures at Input Power Set to 26 dBm

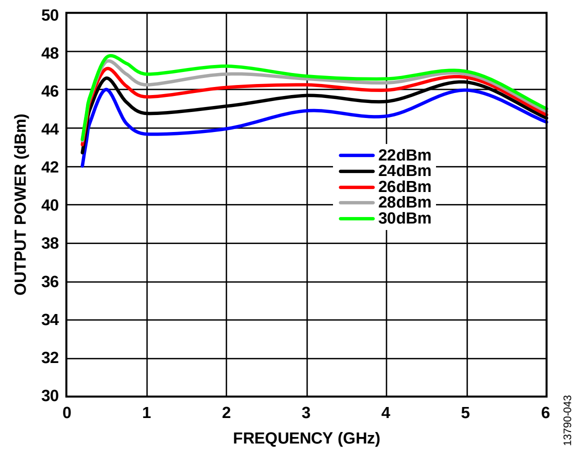

Figure 31. Output Power (P_{OUT}) vs. Frequency at Various Input Powers

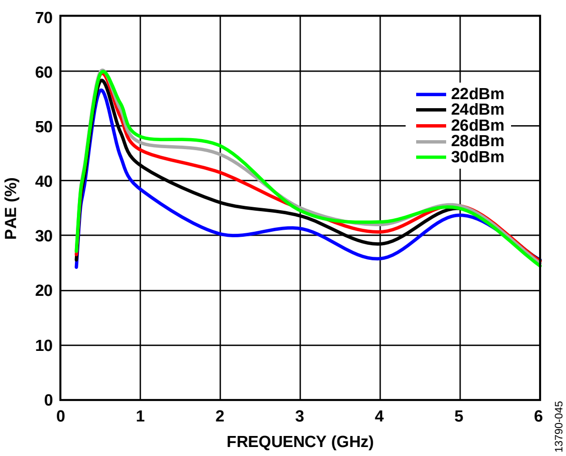

Figure 29. PAE vs. Frequency at Various Input Powers

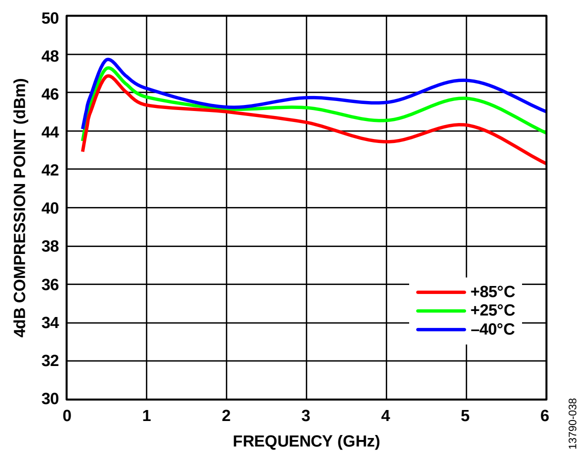

Figure 32. 4 dB Compression Point vs. Frequency at Various Temperatures

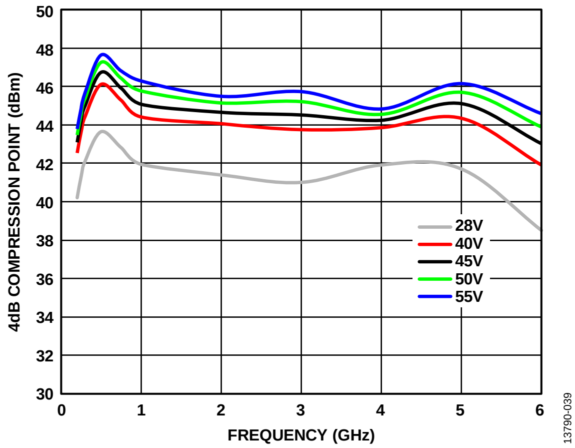

Figure 33. 4 dB Compression Point vs. Frequency at Various Supply Voltages

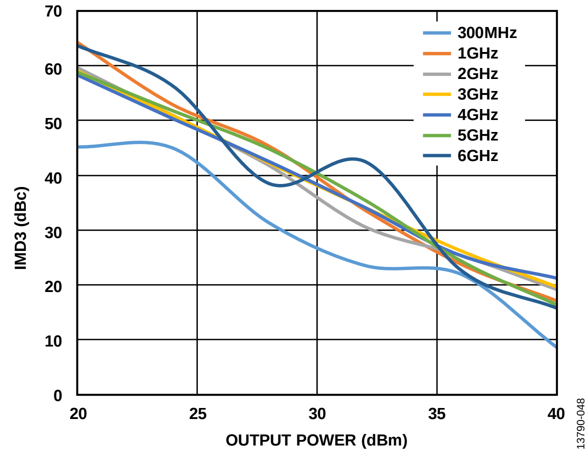

Figure 36. Upper Third-Order Intermodulation (IMD3) vs. Output Power at Various Frequencies

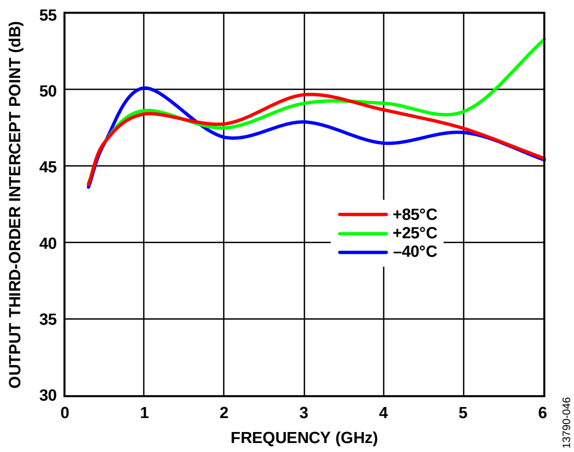

Figure 34. Output Third-Order Intercept Point vs. Frequency at 32 dBm Output Power at Various Temperatures

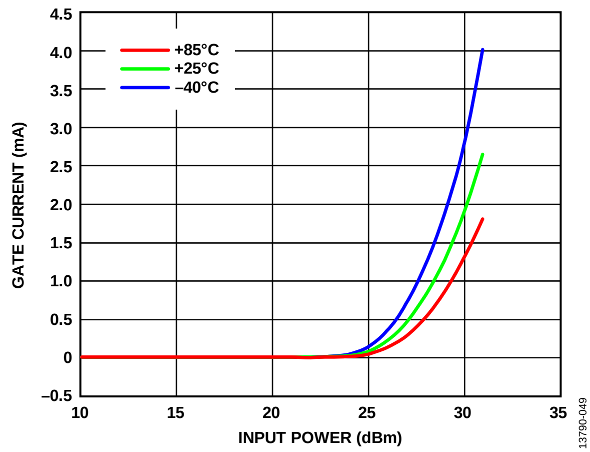

Figure 37. Gate Current vs. Input Power at Various Temperatures

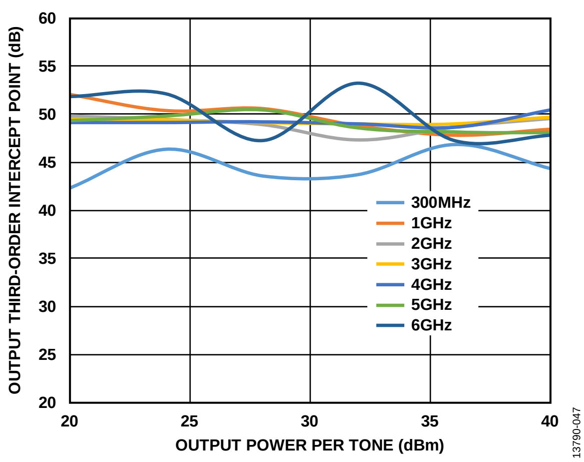

Figure 35. Output Third-Order Intercept Point vs. Output Power per Tone at Various Frequencies

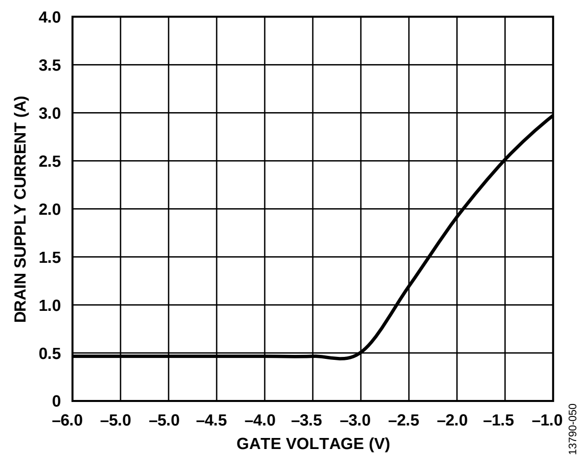

Figure 38. Drain Supply Current vs. Gate Voltage

THEORY OF OPERATION

The HMC8205BF10 is a 35 W, GaN power amplifier consisting of two cascaded gain stages. The first stage requires only a single positive drain supply, which also internally generates gate bias such that a first stage quiescent drain current of approximately 400 mA results for a 50 V drain voltage. The second stage has a distributed architecture that is biased by a separate positive drain supply plus an externally applied negative gate supply. When 50 V is used to bias the first and second stage drains together, adjust the negative voltage applied to $V_{GG}1$ to obtain a total quiescent drain current of 1300 mA.

When biased as previously described, the device operates in Class A/B, resulting in maximum PAE at saturation. The HMC8205BF10 features integrated RF chokes for each drain plus on-chip dc blocking of the RFIN and RFOUT ports. Capacitive bypassing of the bias supplies improves performance and reduces the required external component count.

The HMC8205BF10 is not rated for moisture sensitivity level. It is a nonhermetic, air cavity device, not surface mountable or suitable for use in a solder reflow process. The package body material is Tungsten Copper 85/15.

APPLICATIONS INFORMATION

The first and second stage drain bias voltages are applied via the $V_{DD}1$ and $V_{DD}2$ pins, respectively, and the second stage gate bias voltage is applied via the $V_{GG}1$ pin. A single supply can be used for both drains. Capacitive bypassing of all drain and gate pins is required (see Figure 39). When the HMC8205BF10 is used in a 50 Ω system, external matching components are not required for the RFIN and RFOUT ports.

The following is the recommended power-up bias sequence:

1. Connect to ground.
2. Set $V_{GG}1$ to −8 V to pinch off the second stage drain current, $I_{DD}2$.
3. Set $V_{DD}1$ and $V_{DD}2$ to 50 V ($I_{DD}2$ is pinched off, and the first stage drain current $I_{DD}1$ is approximately 400 mA).
4. Adjust $V_{GG}1$ with a more positive voltage (approximately −2.5 V) until a total quiescent $I_{DQ} = I_{DD}1 + I_{DD}2 = 1300$ mA is obtained.
5. Apply the RF signal.

The following is the recommended power-down bias sequence:

1. Turn off the RF signal.
2. Set $V_{GG}1$ to −8 V to pinch off $I_{DD}2$ ($I_{DD}1$ remains approximately 400 mA).
3. Set $V_{DD}1$ and $V_{DD}2$ to 0 V.
4. Set $V_{GG}1$ to 0 V.

Unless otherwise noted, all measurements and data shown in this data sheet were taken using the evaluation PCB shown in Figure 39. The bias conditions, shown in Table 1 and Table 2, are the operating points recommended to optimize the overall performance of the HMC8205BF10.

Unless otherwise noted, the data shown in the Specifications section was taken using the recommended bias conditions. Operation of the HMC8205BF10 at other bias conditions can provide performance that differs from what is shown in this data sheet. Some applications can benefit from the reduced power consumption afforded by the use of lower drain voltages and/or lower drain currents. To understand the trade-offs between power consumption and performance, see Theory of Operation section.

The evaluation printed circuit board (PCB) provides the HMC8205BF10 (see Figure 39), allowing easy operation using standard dc power supplies and 50 Ω RF test equipment.

APPLICATION CIRCUIT

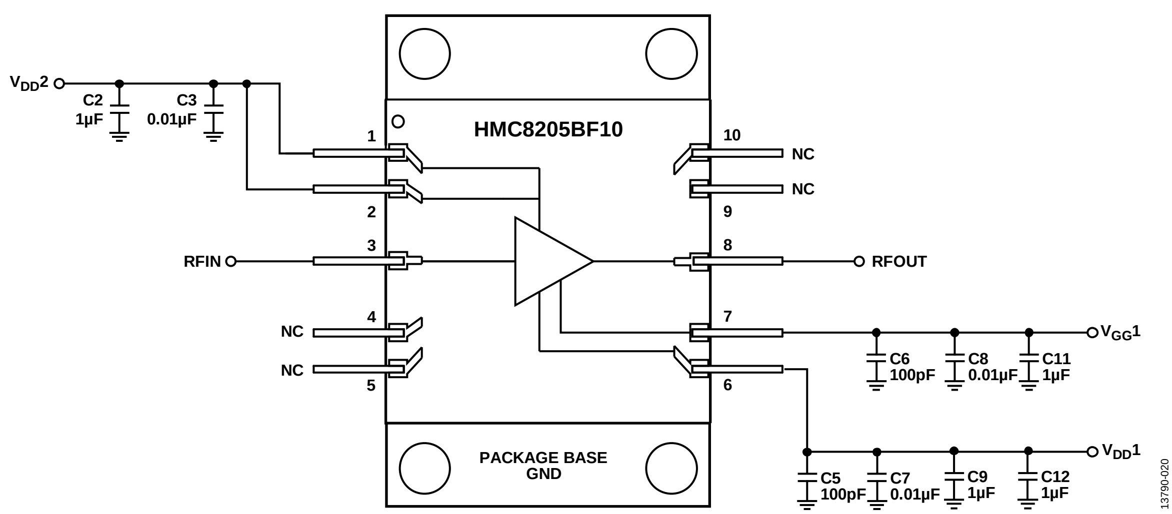

Figure 39. Typical Application Circuit

EVALUATION PCB

Use RF circuit design techniques for the PCB. Provide 50 Ω impedance for the signal lines and directly connect the package ground leads and exposed paddle to the ground plane (see Figure 40). Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation PCB shown in Figure 40 is available from Analog Devices, Inc., upon request. See Table 7 for the bill of materials of the EV1HMC8205BF10.

Table 7. Bill of Materials for Evaluation PCB EV1HMC8205BF10

Reference Designator	Description
RF IN, RF OUT	Subminiature A (SMA) connectors
P1	DC pins
JP1, JP2, JP3	Preform jumpers
C2, C9, C11, C12	1 µF capacitors, 0805 package
C3, C7, C8	0.01 µF capacitors, 0402 package
C5, C6	100 pF capacitors, 0603 package
U1	HMC8205BF10
PCB	EV1HMC8205BF10 Rogers 4350 or Arlon 25FR

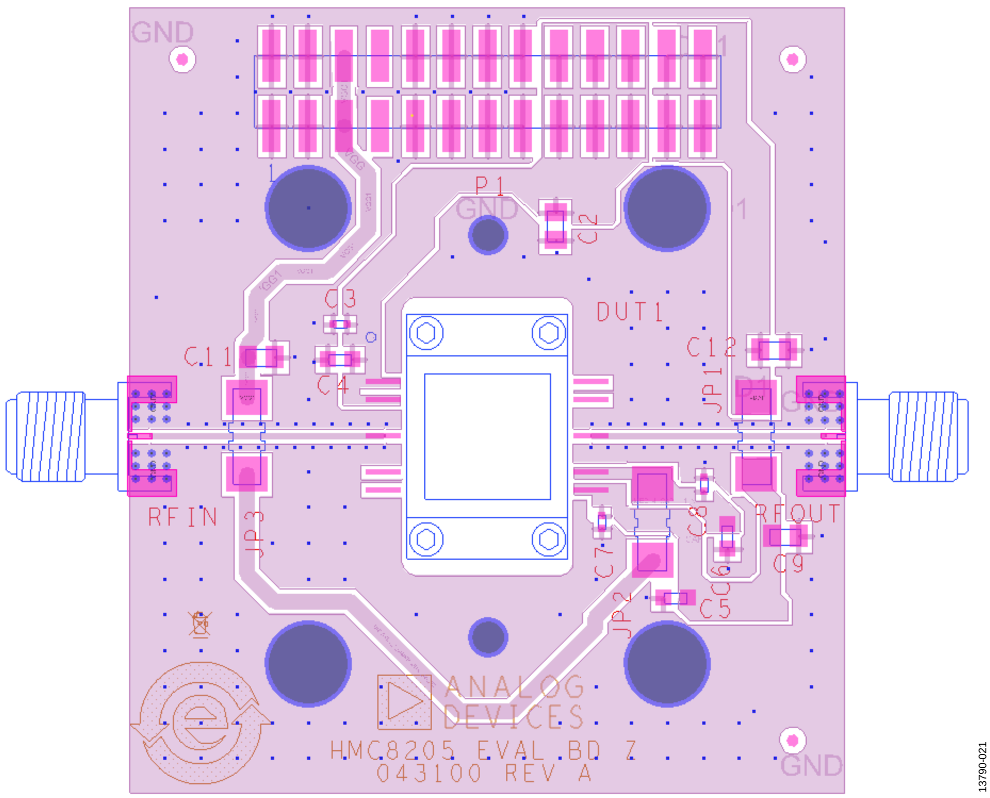

Figure 40. Evaluation PCB

OUTLINE DIMENSIONS

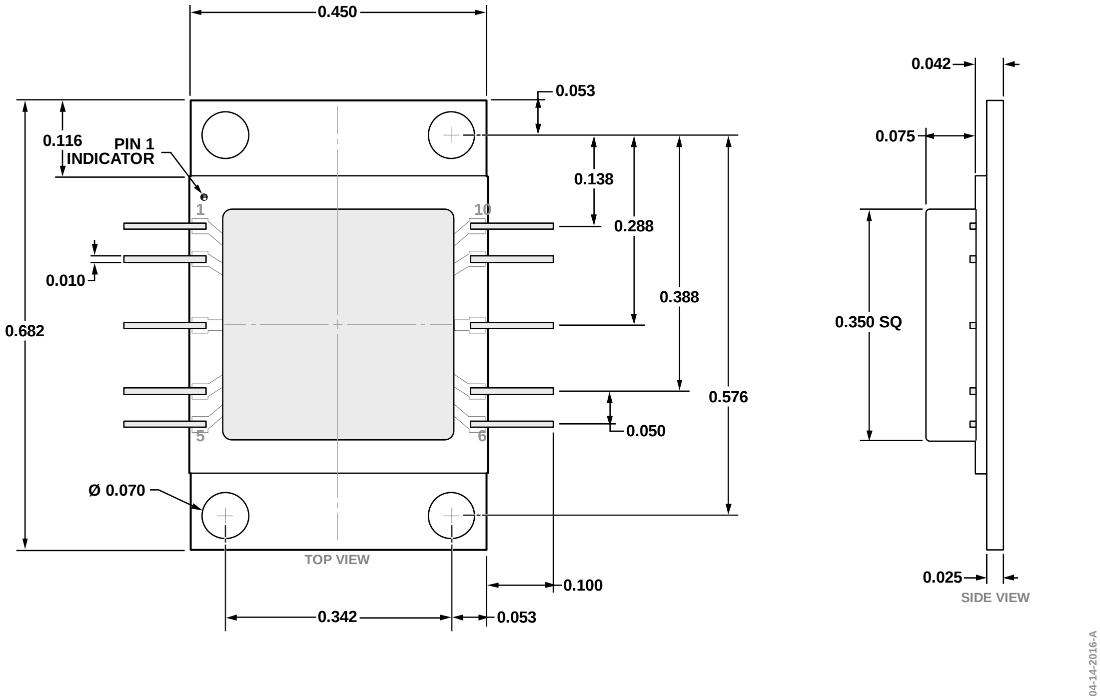

Figure 41. 10-Lead Ceramic Leaded Chip Carrier [LDCC]
(EJ-10-1)
Dimensions shown in inches

ORDERING GUIDE

Model[1]	Temperature	Description	Package Option
HMC8205BF10	−40°C to +85°C	10-Lead Ceramic Leaded Chip Carrier [LDCC]	EJ-10-1
EV1HMC8205BF10		HMC8205BF10 Evaluation PCB	

[1] The HMC8205FB10 is a RoHS compliant device.